Sixth-Order Multi-Bit Delta-Sigma Modulator With 12-Bits

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ABSTRACT

This paper presents sixth-order delta-sigma modulator for 4-bit quantizer with cascade of resonator with multiple feedback (CRFB). The quantization noise suppression is optimized by increasing out-of-band gain (OBG) of the modulator to 6. The modulator signal-to-noise transfer function (STF) and noise transfer function (NTF) are discussed. The NTF zero optimization technique is applied to suppress quantization in the signal band to suppress quantization noise. The CRFB topology allows to utilize multiple feedback digital-to-analog converter (DAC) for higher stability of the modulator. Due to the CRFB topology the STF shows flat response rather than peak in case CIFF. The 0.55-V full scale of the modulator optimized to maximize the signal-to-noise ratio (SNR). The oversampling ratio of the modulator selected to lower to get higher bandwidth advantage with higher SNR of 76-dB with ideal model. The operational amplifier inside the integrator further optimized for higher performance. The open loop DC gain, slew-rate and gani-bandwidth (GBW) simulated to get an estimate of the performance. Due to mismatch of multi-bit quantizer, the modulator performance may be degraded.

Keywords: Noise transfer function, Operational amplifier, Multi-Bit Delta-Sigma, DC Gain

1. INTRODUCTION

An sixth-order multi-bit delta-sigma modulator is modeled and simulated with SNR of 76 dB. The NTF of the modulator optimized with zero optimization technique to reduce the quantization noise from signal band. The complete modulator circuit non-idealities further simulated like limited DC gain, limited slew-rate, thermal noise, and flicker noise. An oversampling ADC is modeled and simulated for signal bandwidth of 20 MHz with OSR of 16 having sampling frequency of 640 MHz. The non-idealities like finite DC gain of operational amplifier and thermal noise of the complete modulator model also simulated. This paper presents a 2-2 discrete-time sturdy multi-stage noise-shaping (SMASH) delta-sigma modulator using source-follower-based open-loop integrators. The resolution of the SMASH delta-sigma modulator is enhanced by eliminating the first-stage quantization noise from the output. Using the proposed source-follower-based open-loop integrator, the operating speed of the modulator is efficiently improved. The prototype delta-sigma modulator fabricated in a 65-nm CMOS process achieves a 75.8-dB dynamic range and 72.9-dB SNDR in a 20-MHz bandwidth. The modulator occupies an active area of 0.34 mm^2, and its total power consumption is 20.4 mW from a 1.2-V supply voltage operating at a 500-MHz clock frequency [1]. A high-linearity Multi-stAge noise SHaping (MASH) 2–2–2 sigma–delta modulator (SDM) for 20-MHz signal bandwidth (BW) was presented. Multi-bit quantizers were employed in each stage to provide a sufficiently low quantization noise level and thus improve the signal-to-noise ratio (SNR) performance of the modulator. Mismatch

noise in the internal multi-bit digital-to-analog converters (DACs) was analyzed in detail, and an alternative randomization scheme based on multi-layer butterfly-type network was proposed to suppress spurious tones in the output spectrum. Fabricated in a 0.18-μm single-poly 4-metal Complementary Metal Oxide Semiconductor (CMOS) process, the modulator occupied a chip area of 0.45mm^2, and dissipated a power of 28.8mW from a 1.8-V power supply at a sampling rate of 320MHz. The measured spurious-free dynamic range (SFDR) was 94dB where 17-dB improvement was achieved by applying the randomizers for multi-bit DACs in the first two stages. The peak signal-to-noise and distortion ratio (SNDR) was 76.9dB at −1 dBFS @ 2.5-MHz input, and the figure-of-merit (FOM) was 126pJ/conv [2]. A 40 MHz-bandwidth (BW) 12-bit delta-sigma modulator (DSM) fabricated in 90 nm CMOS is presented. A noise-free capacitive local feedback scheme is proposed for noise transfer function complex zeros generation. Moreover, the operational transconductance amplifiers (OTAs) are implemented with a current-sharing feedforward technique to largely reduce the power and to boost the gain. With a 960 MHz clock frequency and 1.2 V supply, the modulator achieves 74.4 dB dynamic range and 69.7 dB peak signal-to-noise and distortion ratio (SNDR). The DSM FoM is 0.22 pJ/conv, which is among the lowest of the published moderate resolution DSMs in this high-bandwidth range [3]. A dual-mode second-order reconfigurable quadrature bandpass continuous-time delta-sigma modulator is presented for a low-IF global navigation satellite system receiver to simplify the entire architecture. The proposed modulator is capable of supporting both narrowband of 5-MHz bandwidth (BW) and wideband of 20-MHz BW. An amplifier topology with active feed-forward and antipole-splitting compensation schemes is proposed. The flexible amplifiers in active-RC integrators and preamplifiers in comparators are implemented with power scaling technique to effectively adjust the power consumption for both BWs. A 1-bit digitally switched current digital-toanalog converter structure with gate-leakage compensation and low-latency dynamic element matching is proposed to cover large current variations and mitigate the gate-leakage issue. Digital I/Q self-calibration algorithm is realized to improve the image rejection ratio (IRR). Implemented in 65-nm CMOS, the ΔΣ modulator achieves 67.8-/61.4-dB dynamic range, 65.9-/53.7-dB signal-to-noise-plus-distortion ratio, and >60-dB IRR after calibration across 5-/20-MHz BW with center frequencies of 4/12 MHz, respectively. Powered by a 1.2 V supply, the modulator only consumes 4.2/8.1 mW, resulting in measured figure-of-merits of 0.26/0.51 pJ/conversion step [4]. A third-order continuous-time Delta-Sigma modulator in a 130 nm CMOS technology is presented. It features a 3-bit quantizer with an intrinsic excess loop delay compensation for half a clock cycle. The compensation is performed by means of adapting the reference voltages of the comparators on a sampling-to-sampling base, thus overcoming a power consuming summation of signals in front of the quantizer. Occupying merely 0.086mm 2 , the modulator achieves 66.4 dB SNDR and 74.6 dB DR in a 20 MHz bandwidth using a 640 MHz clock frequency. The power consumption equals 5.1 mW drawn from a 1.2 V supply voltage, which yields a state-of-the-art Walden figure of merit FOM W of 74.7 fJ/conv-step [5].

This paper proposed a 5th order 4-bit quantizer delta-sigma modulator and can achieve signal-to-noise ratio (SNR) of 90 dB for signal bandwidth of 20 MHz. The loop filter topology is cascade of integrator with multiple feedback (CIFB) with out-of-band gain (OBG) of 3 adjusted with full-scale of 850mV. The signal-transfer function (STF) and noise-transfer function (NTF) of the modulator discussed and zeroes of the NTF adjusted at DC for maximum quantization noise suppression. The STF of the modulator shows low-pass behavior. The modulator SNR without NTF zero optimization technique is 90 dB, while with NTF zero-optimization technique is 107 dB. The NTF zero optimization technique reduces the in-band quantization noise and improves the SNR of 17 dB. The zeroes of the NTF lies on the unit circle while poles lies inside the unit circle. NTF zero optimization techniques shifts these zeroes at the DC and suppress the quantization noise in the signal band. The operational amplifiers for the first integrator optimized for higher DC gain, higher slew-rate, and higher unity gain bandwidth. The circuit non-idealities are also simulated in the MATLAB to estimate the performance of the modulator at the circuit implementation. The thermal noise and flicker noise also simulated for the modulator. Finally, the 5th order modulator with four-bit quantizer can achieves SNR of 90 dB with oversampling ratio (OSR) of 16 having sampling frequency 640 MHz.

After the introduction, the second section discuss the design of the modulator design with CIFB structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for design implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A higher order modulator with five integrators inside the loopfilter and four-bit quantizer modeled using Delta-Sigma Toolbox [12]. The cascade of integrator with multiple feedforward (CIFB) topology employed to investigate the performance for higher out-of-band-gain (OBG) of 3. Different oversampling ratio selected to
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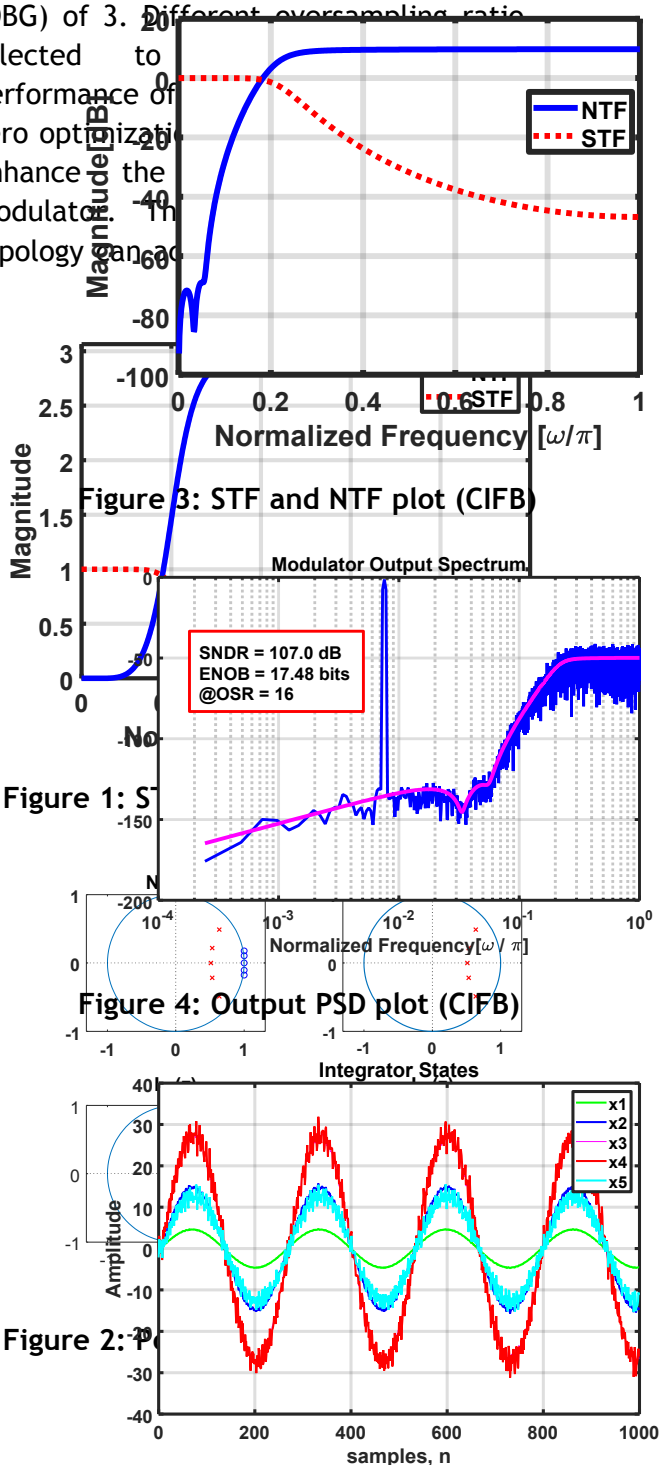

Figure 3: STF and NTF plot (CIFB)

Figure 1: S

Figure 4: Output PSD plot (CIFB)

Figure 2: P

Figure 5: Output states of the integrators

OSR of 16 for signal bandwidth of 20 MHz. The OBG of 3 is selected which much lower for higher stability of the modulator as shown in the Figure 1. The STF, NTF poles and zeroes plots are shown in the Figure 2. All NTF zeroes shows optimized after NTF zero optimization techniques employed. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The signal-transfer function (STF) and noise transfer function (NTF) of the modulator is shown in Figure 3. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 3. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The Figure 4 shows the output power spectral density (PSD) plot with SNR of 107, achieving effective number of bit (ENOB) of 17-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of -145dB, the quantization noise is suppressed maximum with nine integrators inside the loop filter. Due to moderate OSR of 16, the signal bandwidth is 20 MHz. Figure 5 shows that the due to CIFB topology of the modulator the signal swing inside the loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loopfilter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loopfilter.

1. RESULTS & DICUSSION

An oversampling ADC for signal bandwidth of 20 MHz. The loop filter implements CIFB topology the in MATLAB. The modulator can achieve SNR of 107 dB with NTF zero optimization technique. The simulation environment SDToolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A sixth-order multi-bit delta-sigma modulator modeled, and simulation shows it can achieve SNR of 76 dB. To estimate the circuit level performance, complete modulator circuit non-idealities are simulated. It presents sixth-order delta-sigma modulator for 4-bit quantizer with cascade of resonator with multiple feedback (CRFB). The quantization noise suppression is optimized by increasing out-of-band gain (OBG) of the modulator to 6. The modulator signal-to-noise transfer function (STF) and noise transfer function (NTF) are discussed. The NTF zero optimization technique is applied to suppress quantization in the signal band to suppress quantization noise. The CRFB topology allows to utilize multiple feedback digital-to-analog converter (DAC) for higher stability of the modulator. Due to the CRFB topology the STF shows flat response rather than peak in case CIFF. The 0.55-V full scale of the modulator optimized to maximize the signal-to-noise ratio (SNR). The oversampling ratio of the modulator selected to lower to get higher bandwidth advantage with higher SNR of 76-dB with ideal model. The operational amplifier inside the integrator further

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